

Serial No. 10/643,129

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re **PATENT** application of:

Applicant: Timothy M. E. FROST et al.

Serial No.: 10/643,129

Art Unit: 2616

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Confirmation No.: 3518

Title: METHOD AND APPARATUS FOR DISTRIBUTING TIMING DATA
ACROSS A PACKET NETWORK

Examiner: Kevin D. Mew

Docket No.: MARSP0170US

APPEAL BRIEF

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P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is submitted in connection with the appeal of the above-identified application. Credit card payment of the fee set forth in 37 C.F.R. § 41.20(b)(2) is made in connection herewith. If there are any additional fees resulting from this communication, please charge the same to our Deposit Account No. 18-0988, our Docket No. MARSP0170US.

I. Real Party in Interest

The real party in interest in the present appeal is Zarlink Semiconductor Limited, assignee of the present application.

II. Related Appeals and Interferences

Appellants, Appellants' undersigned representative, and/or the assignee of the present application are unaware of any prior or pending appeals, interferences or judicial proceedings which may be related to, directly affect or be directly affected by, or have bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1-10 are in the instant proceeding and are pending in the application. Claims 1-10 stand finally rejected and are the subject of this appeal.

IV. Status of Amendments

No amendments to the claims or the specification have been made subsequent to the final rejection contained in the Final Office Action dated August 21, 2007.

V. Summary of the Claimed Subject Matter

Independent claim 1 recites a method of distributing timing information across a packet network (see generally page 3, lines 18-28 and Figs. 5 and 7). The method comprises, at a master component, generating timing signal packets containing timing signals at predictable intervals using a clock reference of a given frequency (see, e.g., page 6, lines 18-28 and Figs. 4-5), and broadcasting or multicasting the timing signal packets to a plurality of client components over said packet network, preserving the timing signal packet intervals (see, e.g., page 6, line 24 to page 7, line 3 and Figs. 4-5).

The method further comprises, at each said client component, receiving said timing signal packets and determining the intervals between successive packets (see, e.g., page 7, lines 15-20 and Figs. 6-7), applying a clock recovery algorithm to said

determined intervals to recover in substantially real time the original clock frequency, and synchronizing the frequency of a local clock of the client component to the recovered frequency (see, e.g., page 7, lines 15-27 and Figs. 6-7).

Dependent claim 2 recites a method according to claim 1, the method being used to distribute timing information between various components of a telecommunication system coupled together via a packet network (see, e.g., page 3, lines 30-32).

Dependent claim 3 recites a method according to claim 2, wherein said components include one or more components coupled to TDM networks/links (see, e.g., page 3, lines 32-33).

Dependent claim 4 recites a method according to claim 1, wherein one or more of the components is coupled to a T1 or E1, T3 or E3, SONET or SDH link, performing a data conversion function between the T1 or E1, T3 or E3, SONET or SDH data format and the packet network data format (see, e.g., page 3, line 33 to page 4, line 2).

Dependent claim 5 recites a method according to claim 1, the packet network providing a backplane of a telecommunications gateway (see, e.g., page 4, lines 4-5; page 6, lines 12-13 and Fig. 3).

Dependent claim 6 recites a method according to claim 1 and comprising including in said packets, a priority marker, and upon recognition of such packets at routers/switches of the packet network, forwarding them with the highest possible priority (see, e.g., page 4, lines 10-13; page 7, lines 5-11).

Independent claim 7 recites an apparatus for enabling the operating clock frequencies of a plurality of components, coupled to a packet network, to be synchronized to the clock frequency of a master component also coupled to the packet network (see generally page 4, lines 15-29 and Figs. 4 and 6). The apparatus comprises means at the master component for receiving or generating a clock signal having a clock frequency, and for generating from said clock signal, timing signal packets containing timing signals at predictable intervals (see, e.g., page 6, lines 18-28 and Figs. 4-5). The apparatus further comprises means at the master component for

broadcasting or multicasting the timing signal packets to a plurality of client components over said packet network, preserving the timing signal intervals (see, e.g., page 6, line 24 to page 7, line 3 and Figs. 4-5). The apparatus further comprises means at each said client component for receiving said timing signal packets and determining the intervals between successive packets (see, e.g., page 7, lines 15-20 and Figs. 6-7), for applying a clock recovery algorithm to said determined intervals to recover in substantially real time the original clock frequency, and for synchronizing the local clock frequency of the client component to the recovered clock frequency (see, e.g., page 7, lines 15-27 and Figs. 6-7).

Independent claim 8 recites a gateway of a telecommunications network (see generally page 4, line 31 to page 5, line 12 and Fig. 3). The gateway comprises a plurality of components each operating at a local clock frequency, one of the components, the master component, generating or receiving a reference clock signal having a given frequency, and a packet network backplane for communicating packet data between said components (see, e.g., page 6, lines 12-16 and Fig. 3). The master component has means for generating from said clock reference a stream of timing signal packets containing timing signals at predictable intervals (see, e.g., page 6, lines 18-28 and Figs. 4-5), and means for broadcasting or multicasting said timing signal packets, preserving the timing signal packet intervals, to other components operating at said local clock frequencies via said packet network backplane (see, e.g., page 6, line 24 to page 7, line 3 and Figs. 4-5). The receiving components have means for synchronizing their local clock frequencies to said reference clock frequency by analyzing the intervals between received timing signal packets (see, e.g., page 7, lines 15-27 and Figs. 6-7).

Dependent claim 9 recites a gateway according to claim 8, wherein at least one of said components is a TDM line card, coupled in use to a TDM link (see, e.g., page 5, lines 14-15).

Dependent claim 10 recites a gateway according to claim 9, wherein at least one of the components is a TDM line card coupled to a T1 or E1 link whilst at least one

other component is a TDM line card coupled to a T3, E3, SONET or SDH link, the gateway performing up and down conversions for data received and sent via the links (see, e.g., page 3, line 33 to page 4, line 2; page 5, lines 15-19).

VI. Grounds of Rejection to be Reviewed on Appeal

Claims 1-5 and 7-10 stand rejected pursuant to 35 U.S.C. § 102(e) as being anticipated by Dudziak et al., U.S. Patent Application Publication No. 2002/0136232 (*Dudziak et al.*). Claim 6 stands rejected pursuant to 35 U.S.C. § 103(a) as being obvious over *Dudziak et al.* in view of Chang, U.S. Patent Application Publication No. 2003/0020991 (*Chang*).

VII. Argument

Claims 1-5 and 7-10 stand rejected under 35 U.S.C. § 102(e) as being anticipated by on Dudziak et al., U.S. Patent Application Publication No. 2002/0136232 (*Dudziak et al.*). Claim 6 stands rejected under 35 U.S.C. § 103(a) as being obvious over *Dudziak et al.* and a more tertiary reference, Chang, U.S. Patent Application Publication No. 2003/0020991 (*Chang*). Applicants respectfully request withdrawal of the rejections for at least the following reasons.

A. Rejection of Claims 1-5 and 7-10

1. The Claimed Invention and Disclosure of Dudziak et al. Are Fundamentally Different

Independent claims 1, 7, and 8 recite, “at a master component, generating *timing signal packets containing timing signals* at predictable intervals using a clock reference of a given frequency . . .” The claimed invention differs significantly from the teachings of *Dudziak et al.* in that the timing signal information is distributed across the packet network in the form of *timing signal packets* that are broadcast or multicast *over the packet network*. *Dudziak et al.* discloses an arrangement in which timing distribution

takes place by means of transmitted data with *the underlying data signal* carrying the timing information. Thus, *Dudziak et al.* distributes timing information *under the packet network*, i.e., embedded within the data transmission. These two techniques are different, and *Dudziak et al.* does not disclose the distribution of timing signals over a packet network by means of broadcasting or multicasting timing signal packets.

As further shown below, there is a fundamental difference between the claimed invention and what is disclosed in *Dudziak et al.* Referring to claim 1 as representative, claim 1 recites sending timing signal packets at predictable intervals from the master component and, at the client component, regenerating the clock by applying a clock recovery algorithm to the intervals between receipt of successive packets. These features of claim 1 are neither disclosed nor suggested by *Dudziak et al.*, which discloses a substantially different synchronization technique.

2. *Dudziak et al. Teaches Synchronizing the Telecom Clocks to Otherwise Free Running Data Signal Clocks*

Dudziak et al. teaches synchronization of elements of a packet network by synchronizing telecommunication clocks to the *data transmission clock* in each node of a packet network. Thus, each data transmission clock is locked to the telecommunication clocks and is no longer free running, as would be typical.

Figs. 2 and 3 of *Dudziak et al.* are reproduced below, which depict both the synchronization problem and the solution of *Dudziak et al.*

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Conventional Packet Network

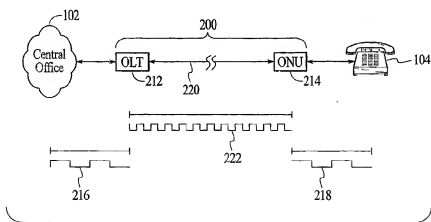


FIG. 2

Dudziak et al.'s Packet Network

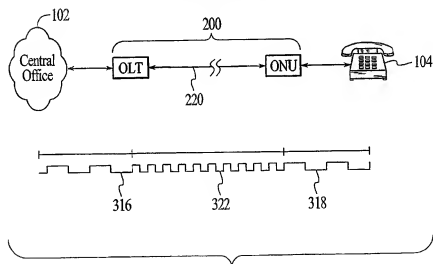


FIG. 3

Dudziak et al. describes its Fig. 2 as depicting a conventional packet network. As seen in Fig. 2, an optical line terminal (OLT) has a telecommunication clock 216, and an optical network unit (ONU) has a telecommunication clock 218. For proper communication, the OLT telecommunication clock 216 and the ONU telecommunication clock 218 must be synchronized. In Fig. 2, the lack of synchronization is depicted by the broken space between clocks 216 and 218. In addition, the network also may have an independent or free running data transmission clock 222, which "is independent from the other clocks of the network" and "would not typically be synchronized to the telecom clocks 216 and 218, as illustrated in Fig. 2." (Paragraph [0027].)

As described in *Dudziak et al.*, therefore, conventional packet networks of this type make use of free running data transmission clocks to time individual bits of the data which are distributed by the network. In a conventional packet network, any telecommunication clock is not linked or synchronized in any way to the underlying data transmission clock, which is free running.

Dudziak et al. attempts to overcome the lack of synchronization of the telecommunication clocks by synchronizing the telecommunications clocks to the data transmission clock in each node of the packet network. This is a departure from the typical configuration, described above, in which the data transmission clock is free running. As further stated in paragraph [0027]: "The Ethernet-based PON System 100 economically solves the problem of telecom clock synchronization by utilizing a data transmission clock 222 that is used to time the transmission of data between the OLT 212 and the ONU . . . The ONU then extracts the timing information from the transmitted data to generate the telecom clock 218, which is synchronized with the telecom clock 216 of the OLT. In other words, the telecom clock 218 of the ONU is synchronized with the data transmission clock 222, which in turn is synchronized with the telecom clock 216 of the OLT." This is depicted in Fig. 3 of *Dudziak et al.*, reproduced above, as shown by the interconnection of the lines representing the telecommunication clocks 316 and 318 with that of the data transmission clock 322.

Thus, each data transmission clock is locked to the telecommunication clocks, and is no longer free running.

In this vein, the Examiner relies on paragraphs [0032-0035] of *Dudziak et al.* in his rejections, but these paragraphs merely provide details as to how the OLT and ONU telecommunications clocks are synchronized to the data transmission clock. Fundamentally, however, this method of synchronization bears no similarity to the manner of distributing timing information of the claimed invention.

3. The Claimed Invention, In Contrast, Recites Broadcasting or Multicasting Timing Signal Packets Independent of Any Data Transmission

In contrast to the method of *Dudziak et al.*, the present invention involves distributing timing information in the form of intervals between timing signal packets, and not by means of relating the timing signals to the bit rate of the data transmission. In other words, the distributed timing information is not, in any way, related to the data transmission rate. The timing information is not synchronized with any data transmission clock, and the data transmission clocks remain independent and free running similar to the manner depicted in Fig. 2 of *Dudziak et al.* above.

Fig. 3 of the application is reproduced below. As can be seen, timing signal packets 14 are generated from the master component 8, and broadcasted or multicasted to the client components 9. The timing signal packets are discreet units of timing information, and are independent of any data transmission. Comparing this Fig. 3 of the application to Fig. 3 above of *Dudziak et al.*, the differences are readily apparent. As seen in Fig. 3 of *Dudziak et al.*, the timing clocks 316 and 318 are linked to or embedded within the data clock 322. *Dudziak et al.* does not disclose that the timing information is broadcasted or multicasted in independent packets, as shown in Fig. 3 of the application below.

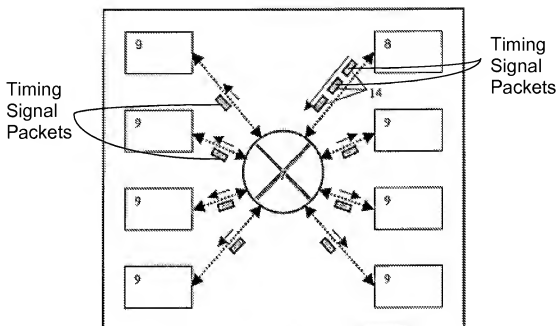


Figure 3
Application

Thus, the timing signal packets are independent and discreet units of information. These timing packets are recited in each of the independent claims. According to independent claims 1, 7, and 8, the master component generates "timing signal packets at predictable intervals". Such intervals are not related to the data transmission rate or clock in any fashion (in contrast to *Dudziak et al.*). The manner of generation of the timing signal packets at predictable intervals is described in the application at page 6, third paragraph of the Detailed Description. The timing signal packets are then broadcasted or multicasted to the client components.

Also as claimed, the receiving terminals "determine the intervals between successive [timing signal] packets, applying a clock recovery algorithm to said

determined intervals to recover in substantially real time the original clock frequency, and synchronizing the frequency of a local clock of the client component to the recovered frequency.” Thus, at the receiving terminal, the timing information is regenerated by using an algorithm based on the timing of arrival of the timing signal packets which, again, is not related to or synchronized with the data transmission rate. The claimed invention, therefore, may recover or distribute timing information across any packet network, going across several nodes that are not synchronized with each other, whereas *Dudziak et al.* is limited to the use of networks in which all of the nodes work with data transmission rates which are synchronized with each other.

In other words, by broadcasting or multicasting timing signal packets, a client component may receive the timing information whether or not the client receives any data transmission. It appears that in the method of *Dudziak et al.*, a client component that does not receive a data transmission also would not receive any timing information. The claimed invention, therefore, can provide timing synchronization in a greater number of packet networks, and/or to a greater breadth of client components, as compared to the method disclosed by *Dudziak et al.*

The claimed invention has an intrinsic and major advantage over the technique disclosed by *Dudziak et al.* In particular, the claimed technique does not require every node in a network to participate in the clocking scheme. Thus, timing information may be distributed across any packet network, and in particular through, for example, legacy Ethernet networks. The technique according to *Dudziak et al.* cannot be used efficiently in legacy networks because it would require every node in the network to be modified in order to work at all.

For at least these reasons, the system of *Dudziak et al.*, by which each of the OLT and ONU telecommunication clocks are synchronized to a data transmission clock, lacks the features of the independent claims in at least the following respects.

- (1) A master component does not generate “timing signal packets” at all.
- (2) A master component does not generate “timing signal packets at predictable

intervals".

(3) By virtue of (1) and (2), timing signal packets are not broadcasted or multicasted to a plurality of client components.

(4) At the client components, there is no "determining the intervals between successive [timing signal] packets".

(5) Nor is there "applying a clock recovery algorithm to said determined intervals to recover in substantially real time the original clock frequency, and synchronizing the frequency of a local clock of the client component to the recovered frequency."

In the Final Office Action and the Advisory Action, the Examiner additionally relies on paragraph [0009] of *Dudziak et al.*, which references "transmitting data in variable-length packets".¹ Although *Dudziak et al.* does make reference to the transmission of variable-length data packets, this reference is an entirely general description of a conventional packet network, and is not in any way related to clock synchronization. The Examiner appears to be arguing that the embedding of the timing information within a data packet creates a timing signal packet, which is not correct.

Particularly in the Advisory Action, the Examiner references the "sequence of ticks" that may be derived from a reference clock by dividing, which he concludes is comparable to what is disclosed in *Dudziak et al.* The Examiner misinterprets the "ticks" as being the actual transmission time. Rather, the sequence of ticks is used to generate and transmit timing signal packets, while the actual time of transmission is determined by the local clock using the recovery algorithm. In the present invention, the local clock need not be synchronized to anything, which differs from the disclosure of *Dudziak et al.* in which the local telecom clocks must be synchronized to the data transmission clocks. The Examiner's reliance on paragraph [0009], therefore, lacks merit.

For at least these reasons, *Dudziak et al.* does not teach the invention as recited in claims 1, 7, and 8. For the same reasons, *Dudziak et al.* does not teach or suggest the features of the various dependent claims. Applicants, therefore, respectfully

¹

This paragraph appears to be misidentified as paragraph 0005 in the Advisory Action.

request withdrawal of the rejections.

B. Rejection of Claim 6

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being obvious over *Dudziak et al.* in view of *Chang*. *Chang* is cited as disclosing only the specific features of claim 6 relating to priority markers. *Chang* does not make for the deficiencies of *Dudziak et al.* as to the base claim 1, from which claim 6 depends. Accordingly, a combination of *Dudziak et al.* and *Chang* does not result in or disclose the invention of claim 6.

C. Conclusion

For at least these reasons, claims 1-5 and 7-10 are not anticipated by *Dudziak et al.*, and for the same reasons, claim 6 is not obvious over *Dudziak et al.* in view of *Chang*. Accordingly, Appellants respectfully request reversal of the Examiner's rejections of claims 1-10.

VII. Claims Appendix

An appendix containing a copy of the claims involved in this appeal is attached to this brief.

IX. Evidence Appendix

An evidence appendix is attached, but identifies no items of evidence.

X. Related Proceedings Appendix

A related proceedings appendix is attached, but identifies no decisions.

Respectfully submitted,

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CLAIMS APPENDIX

1. A method of distributing timing information across a packet network, the method comprising:
at a master component, generating timing signal packets containing timing signals at predictable intervals using a clock reference of a given frequency, and broadcasting or multicasting the timing signal packets to a plurality of client components over said packet network, preserving the timing signal packet intervals; and
at each said client component, receiving said timing signal packets and determining the intervals between successive packets, applying a clock recovery algorithm to said determined intervals to recover in substantially real time the original clock frequency, and synchronizing the frequency of a local clock of the client component to the recovered frequency.
2. A method according to claim 1, the method being used to distribute timing information between various components of a telecommunication system coupled together via a packet network.
3. A method according to claim 2, wherein said components include one or more components coupled to TDM networks/links.
4. A method according to claim 1, wherein one or more of the components is coupled to a T1 or E1, T3 or E3, SONET or SDH link, performing a data conversion function between the T1 or E1, T3 or E3, SONET or SDH data format and the packet network data format.
5. A method according to claim 1, the packet network providing a backplane of a telecommunications gateway.

6. A method according to claim 1 and comprising including in said packets, a priority marker, and upon recognition of such packets at routers/switches of the packet network, forwarding them with the highest possible priority.

7. An apparatus for enabling the operating clock frequencies of a plurality of components, coupled to a packet network, to be synchronized to the clock frequency of a master component also coupled to the packet network, the apparatus comprising:

means at the master component for receiving or generating a clock signal having a clock frequency, and for generating from said clock signal, timing signal packets containing timing signals at predictable intervals;

means at the master component for broadcasting or multicasting the timing signal packets to a plurality of client components over said packet network, preserving the timing signal intervals; and

means at each said client component for receiving said timing signal packets and determining the intervals between successive packets, for applying a clock recovery algorithm to said determined intervals to recover in substantially real time the original clock frequency, and for synchronizing the local clock frequency of the client component to the recovered clock frequency.

8. A gateway of a telecommunications network, the gateway comprising:

a plurality of components each operating at a local clock frequency, one of the components, the master component, generating or receiving a reference clock signal having a given frequency; and

a packet network backplane for communicating packet data between said components,

the master component having means for generating from said clock reference a stream of timing signal packets containing timing signals at predictable intervals, and means for broadcasting or multicasting said timing signal packets, preserving the timing signal packet intervals, to other components operating at said local clock frequencies

via said packet network backplane, and the receiving components having means for synchronizing their local clock frequencies to said reference clock frequency by analyzing the intervals between received timing signal packets.

9. A gateway according to claim 8, wherein at least one of said components is a TDM line card, coupled in use to a TDM link.

10. A gateway according to claim 9, wherein at least one of the components is be a TDM line card coupled to a T1 or E1 link whilst at least one other component is a TDM line card coupled to a T3, E3, SONET or SDH link, the gateway performing up and down conversions for data received and sent via the links.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.